METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to a method of manufacturing a semiconductor device which can prohibit generation of a TED (transient enhanced diffusion) phenomenon of a dopant implanted into the bottom structure and prevent degradation of the film quality at the upper side due to outgasing, in a subsequent annealing process after an ion implantation process is implemented.

Background of the Related Art

In order to manufacture the semiconductor device, it is required that the ion implantation process as well as the deposition process and the etch process be necessarily implemented.

In general, in order to manufacture the flash memory device or the transistor, a well region is formed by means of the ion implantation process. An ion implantation layer for controlling the threshold voltage is then formed at a given depth of the well. Next, before a pad nitride film is formed, a tunnel oxide film and a first polysilicon layer for forming a floating gate is formed and is then patterned.

Thereafter, a semiconductor substrate between the first polysilicon layers is etched to form a trench. A wall sacrificial oxidation process and a well oxidation process are then sequentially implemented to form an isolation film by means of a SA-STI (self-aligned shallow trench isolation) method for electrically isolating the devices.

In the above, in case of a date flash device using an nMOS transistor as a cell, boron (B) is implanted to form an ion implantation layer for adjusting the threshold voltage. At this time, as the cell is programmed and erased in a sector program/erase mode of 512byte unit in the date flash device, it is required that the threshold voltages of the cells be uniform within the unit cell block.

Of them, as the date flash of the flash devices employs a mode using FN tunneling not HCE (hot carrier effect) as a program mode, distribution of a dopant implanted in order to control the threshold voltage becomes an important parameter unlike from the code flash in which formation of the depletion region is important. For this reason, it is required that distribution of the ion implantation layer be not changed even in a subsequent annealing process within the effective channel length, than that the operation speed depending on the driving voltage is increased by the ion implantation layer for controlling the threshold voltage.

If the isolation film is formed by the SA-STI method, however, transient enhanced diffusion (TED) of the dopant occurs at the high temperature oxidization process, which changes the threshold voltage of the device. Furthermore, if a dopant of a large mass is implanted in order to

adjust the threshold voltage of the device, fail may happen by means of RDG (remained dopant gettering) that may occur due to the dopant of the large mass. Therefore, in order to minimize damage caused by ion implantation, high temperature annealing must be implemented as a subsequent process. For this reason, the dopant of the large mass could not be used as an ion for controlling the threshold voltage.

In addition, in case of BF_2 being a dopant that has been widely used in order to form a shallow effective channel region of a surface channel, dopant loss occurs due to outgasing by a subsequent annealing process. In particular, in the cell necessarily requiring the high temperature process, F induced outgasing is inevitable due to maximized outgasing of F. Due to this, there is a problem that the film quality of the oxide film is degraded.

SUMMARY OF THE INVENTION

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method of manufacturing semiconductor devices capable of prohibiting by maximum generation of a TED (transient enhanced diffusion) phenomenon of a dopant and preventing degradation of the film quality due to outgasing, in an annealing process for mitigating damage caused by ion implantation, in a manner that an atomic dopant having a large atomic weight and made of monoatomic is implanted to form an ion implantation layer, instead of using a dopant of a small atomic weight such as B or a molecular ion such as a BF_2

which has been usually employed, in case that the ion implantation layer is formed in order to control the threshold voltage of the semiconductor device.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of manufacturing semiconductor devices according to the present invention is characterized in that it comprises the steps of providing a semiconductor substrate for which given processes for forming the semiconductor device are implemented, and implanting a 3 balance dopant having a higher atomic weight than boron and made of monoatomic at a given depth of the semiconductor substrate by means of an ion implantation process, thus forming an ion implantation layer.

In the above, the dopant may be implanted with a screen oxide film formed.

The ion implantation process includes implanting a dopant of 5E11 ~ 1E13ion/cm^2 with energy of 10 ~ 50KeV. The dopant may be indium. Further, the ion implantation process may include implanting the dopant at a tilt angle of 3 ~ 13° .

Furthermore, a rapid thermal process may be implemented in order to activate the dopant after the ion implantation layer is formed. At this time, the rapid thermal process may be implemented at a temperature of 800 ~ 1100℃ at the ratio of 20 ~ 50 ℃/sec for 5 ~ 30 seconds. Also, the raid thermal process may be implemented under a nitrogen atmosphere.

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

FIG. 1A ~ FIG. 1E are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

FIG. 1A ~ FIG. 1E are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device according to a preferred embodiment of the present invention.

Referring to FIG. 1A, a screen oxide film **102** is formed on a semiconductor substrate **101** as a sacrificial oxide film for crystal defect prohibition or surface treatment of the surface of the semiconductor substrate **101**. The screen oxide film **102** also serves to prohibit inter-diffusion by channeling of the dopant that occurs in the ion implantation process for forming the well. In the above, the screen oxide film **102** is formed in a dry or wet oxidization mode at a temperature of 750 ~ 800℃ and is formed in thickness of 70 ~ 100Å.

Meanwhile, a cleaning process may be implemented before the screen oxide film **102** is formed. At this time, the cleaning process may be implemented by sequentially using hydrofluoric acid (DHF) where H_2O:HF are mixed in the ratio of 50:1 ~ 100:1 and a SC-1($NH_4OH/H_2O_2/H_2O$) solution, or sequentially using BOE (buffered oxide etchant) in which a solution where NH_4F:HF is mixed in the ratio of 4:1 ~ 7:1 is diluted into H_2O in the ratio of 1:100 ~ 1:300 and the SC-1($NH_4OH/H_2O_2/H_2O$) solution.

Referring to FIG. 1B, a triple n well **103** is formed on a region where an n channel will be formed by means of the ion implantation process. A p well **104** is consecutively formed in depth shallower than the triple n well **103**. In the above, the triple n well **103** may be formed by implanting P of 5E12 ~ 5E13ion/cm^2 with energy of 500 ~ 2000KeV. The p well **104** may be formed by implanting B of 1E12 ~ 5E13ion/cm^2 with energy of 200 ~ 1000KeV.

Meanwhile, an n well (not shown) is formed in another region where a p channel device is to be formed. The n well may be formed by implanting P of 1E12 ~ 5E13ion/cm^2 with energy of 200 ~ 1000KeV. In the above, it is preferred that the ion implantation process for forming the well is implemented at a tilt angle of 3 ~ 13° for the purpose of prohibiting dopant channeling.

By reference to FIG. 1C, an ion implantation layer **105** for controlling the threshold voltage is formed at a given depth of the p well **104** by means of the ion implantation process in order to control the threshold voltage of the semiconductor device that will be formed in the semiconductor substrate **101** in a subsequent process. In the above, the ion implantation layer **105** is formed by implanting atomic dopant having a high atomic weight and made of monoatomic, instead of using a dopant having a low atomic weight such as B and a molecular ion such as BF_2 as a dopant that was conventionally used. For example, the ion implantation layer **105** may be formed by implanting 3 balance dopant having a higher atomic weight than boron and made of monoatomic, preferably indium. At this time, the ion implantation process may be implemented using a dopant of 5E11 ~ 1E13ion/cm^2 with energy of 10 ~ 50KeV. Meanwhile, like the ion implantation process for forming the well, even when the ion implantation process for controlling the threshold voltage is implemented, it is preferred that ion implantation is implemented at a tilt angle of 3 ~ 13° in order to prohibit dopant channeling of the channel region in a date flash using a buried channel.

Immediately after the ion implantation layer **105** for controlling the threshold voltage is formed, an annealing process capable of minimizing

exposure at high temperature such as RTP (rapid thermal process is implemented in order to maximize dopant activation. Only activation of the dopant may be maximized while preventing unnecessary rediffusion of the dopant. At this time, the annealing process may be implemented at a temperature of 800 ~ 1100℃ for 5 ~ 30 seconds in the rate of 20 ~ 50℃/sec. Further, the annealing process may be implemented under nitrogen atmosphere in order to prevent formation of a native oxide film.

Referring to FIG. 1D, after the screen oxide film (**102** in FIG. 1C) is removed, a gate oxide film (tunnel oxide film **106** in case of the flash device), a conductive material layer **107** and a pad nitride film **108** are sequentially formed.

In the above, the screen oxide film (**102** in FIG. 1C) is removed by a cleaning process sequentially using hydrofluoric acid (DHF) where H_2O:HF is mixed in the ratio of 50:1 ~ 100:1 and SC-1($NH_4OH/H_2O_2/H_2O$) solution.

Thereafter, the gate oxide film **106** is formed by a wet oxidization process at a temperature of 750 ~ 800℃. The gate oxide film **106** is then annealed under nitrogen atmosphere at a temperature of 900 ~ 910℃ for 20 ~ 30minutes in order to minimize an interface defect of the semiconductor substrate **101** and the gate oxide film **106**.

Meanwhile, the conductive material layer **107** may be formed by depositing a doped polysilicon layer the grain size of which is minimized, by means of a LP-CVD (low pressure chemical vapor deposition) method using SiH_4 or Si_2H_6 and PH_3 gas at a temperature of 580 ~ 620℃ under a low pressure of 0.1 ~ 3Torr. At this time, the impurity (P) concentration of the

doped polysilicon layer is controlled to be a level of 1.5E20 ~ 3.0E20 atoms/cc and the doped polysilicon layer is formed in thickness of 250 ~ 500 Å.

The pad nitride film **108** formed on the conductive material layer **107** may be formed in thickness of 900 ~ 2000 Å by means of the LP-CVD method.

Referring to FIG. 1E, the pad nitride film **108**, the conductive material layer **107** and the gate oxide film **106** in the isolation region are sequentially removed by means of an etch process, thus exposing the semiconductor substrate **101** in the isolation region. Next, the exposed semiconductor substrate **101** in the isolation region is etched by a given depth to form a trench **109**. The trench **109** is then buried with an insulating material (not shown) to form an isolation film (not shown) of a STI (shallow trench isolation) structure. In the above, a high density plasma (HDP) oxide film may be used as the insulating material. At this time, the high density plasma (HDP) oxide film is formed in thickness of 4000 ~ 10000 Å on the entire structure so that the trench **109** is completely buried while preventing generating of void.

Although not shown in the drawings, a chemical mechanical polishing process as a subsequent process is continuously implemented so that the insulating material remains only up to a target height rather than the surface of the semiconductor substrate **101** while removing the insulating material on the pad nitride film **108**. Next, after a wet cleaning process using diluted HF is implemented, a material same to the conductive material **107** is formed in thickness of 400 ~ 1000 Å. A common process of manufacturing the flash memory cell is implemented to complete the flash memory cell.

As described above, the present invention has the following effects through the method of manufacturing the semiconductor devices:

First, in the memory cell of the date flash device in which the isolation film of the STI structure requiring frequent high temperature process must be formed, atomic dopant having a high atomic weight and made of monoatomic is implanted to form an ion implantation layer for controlling the threshold voltage. Therefore, the device could be fabricated while minimizing the TED phenomenon.

Second, the uniformity of the threshold voltage could be secured within the target range while minimizing the TED phenomenon. Therefore, program/erase operation characteristics of a cell block unit could be improved in the flash memory device.

Third, after the ion implantation layer is formed, there is no outgasing in the course of implementing a subsequent annealing process. It is thus possible to prevent degradation of the film quality of the gate oxide film.

Fourth, it is possible to form the gate oxide film of a high quality by preventing degradation of the film quality of the gate oxide film. Accordingly, it is possible to improve electrical characteristics and reliability of the date flash memory device using FN tunneling.

Fifth, as dopant damage due to out diffusion is minimized, it is possible to control the threshold voltage with minimum ion implantation. Furthermore, as generation of ion implantation damage within the channel region is prohibited, it is possible to minimize generation of the leakage current.

The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.